Implementation and Switching Behavior of a PCB-DBC IGBT Module Based on the Power Chip-on-Chip 3D Concept

Jean-Louis Marchesini, Pierre-Olivier Jeannin, Yvan Avenas, Johan Delaine, Cyril Buttay, Raphaël Riva

Implementation and Switching Behavior of a PCB-DBC IGBT Module Based on the Power Chip-on-Chip 3D Concept

Jean-Louis Marchesini, Pierre-Olivier Jeannin, Yvan Avenas, Johan Delaine
Univ. Grenoble Alpes, G2Elab, F-38000 Grenoble, France
CNRS, G2Elab, F-38000 Grenoble, France
Pierre-Olivier.Jeannin@g2elab.grenoble-inp.fr
Yvan.Avenas@g2elab.grenoble-inp.fr

Cyril Buttay, Raphaël Riva
Université de Lyon F-69622, France
CNRS, UMR5005, INSA Lyon, Laboratoire Ampere F-69621
Villeurbanne, France

***Abstract*—With the emergence of new power semiconductor devices, the switching speeds in power converters are increasing. The stray inductances of switching cells must therefore be minimized to limit over-voltages on transistors. One relatively new approach, called Power Chip-on-Chip (PCoC), considers the integration of power dies, one on top of the other, directly in the busbar. This allows for the reduction of the stray inductance. This paper first presents the implementation of a PCoC module using classical packaging techniques. Then a description of the different technological steps for the realization is outlined. Finally, experimental characterization results confirm the lower stray inductances offered by the PCoC package compared with the planar one.**

I. INTRODUCTION

Due to the emergence of new power SiC [1] or GaN semiconductor devices, the switching speeds are continually increasing. This evolution leads to important issues like over-voltages (Fig. 1), EMI coupling and common mode currents. Classically, power module technology is based on a planar (2D) concept [2]. This technology is mature, well mastered and cost-effective, but one of the main drawbacks is that the total internal stray inductance of the module is significant and can reach several tens of nH [3-4]. This relatively high value is due to wire bonding, to substrate tracks and principally to terminal connections. Voltage ratings of power semiconductors are thus traditionally overrated to withstand the voltage spikes due to this large stray inductance value. With new high speed components, this value becomes critical. Indeed with GaN HEMT the stray inductance must be limited to a few nH to take advantage of these components in term of commutation speed. One way to reduce the stray inductance is to place the dies very close to each other in order to decrease the length of the current path. However this configuration induces some drawbacks for the thermal management. This is the reason why 3D packaging is today the subject of intense researches. In fact, classical 3D concepts aim to reduce the stray inductances and to improve the thermal management by a possible extraction of the heat flux from both sides of the dies [5-6].

Several years ago, a new concept called Power Chip-on-Chip was presented [7]. This concept is based on the global integration of the semiconductor devices as close as possible to the busbar to improve the electrical and electromagnetic behavior of the module. The switching cell is sandwiched between two copper plates which are linked to the DC bus (Fig. 2). This structure has several advantages [7]:

- the stray inductance is minimized, even compared to more classical 3D approaches due to the global integration as part of the busbar itself [8],
- the common mode current due to the power module structure can also be significantly reduced [9],
- the radiated EMI are confined in the stack because the $+V_{DC}$ and $-V_{DC}$ copper plates act as magnetic shields,
- decoupling capacitors can also be integrated directly in the stack to reduce the current path,
- the inductive coupling between the gate circuit and the power circuit is reduced by integrating the gate driver connection in the central copper plate.

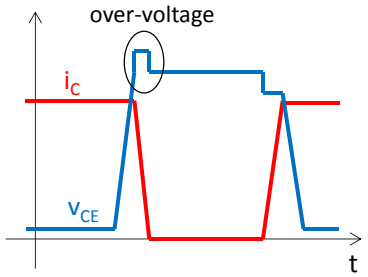


Figure 1. Simplified IGBT switching waveforms

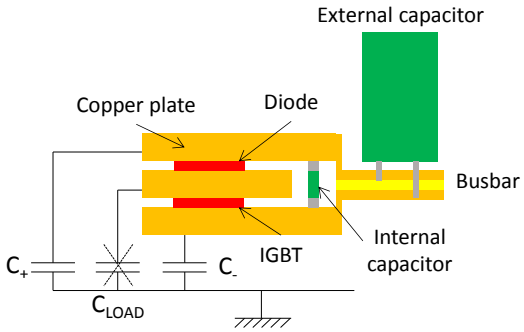


Figure 2. The Power Chip-on-Chip concept [8].

The previous results on PCoC structures were obtained on simplified test structures which cannot be used in real conditions. In fact, [7] and [8] present structures which are based on a stack of copper plates and chips (Fig. 2) maintained by an external pressure. They present therefore several drawbacks:

-the connection of the gate circuit to the IGBT chip is very challenging,

-the antiparalleling of diode and IGBT chips to realize bidirectional switches is difficult due to their different thicknesses,

-the integration of DC link decoupling capacitors is complicated,

-an external clamping system is required to hold the stack together.

Concerning the last point, it has to be noted that commercial products including SMD capacitors in planar packages are available. For example, the 10-PZ126PA080ME-M909F18Y power module from Vincotech (SiC MOSFETs) uses such capacitances to reduce the stray inductance. Some research groups also work on the integration of decoupling capacitance in 3D power modules. For example it can be directly integrated inside the PCB [10]. It is therefore necessary to integrate decoupling capacitors in the PCoC module to study their influence on the stray inductance of the switching cell.

The objective of this paper is thus to introduce a new module structure implementing the PCoC concept, using mature technologies and integrating decoupling capacitors. Sections II and III of this paper describe the principle and the integration steps of this PCoC module. In section IV, the module is characterized in terms of stray inductance value and compared to a planar module. Then, the results are analyzed in section V.

II. Principle of the PCoC Module Implementation

To reduce the stray inductance, the PCoC module implementation must be based on new technologies developed for bondwire free solutions. Numerous research groups have studied such power modules. A brief overview is given in the following paragraph.

A. Literature overview

Today, the most advanced solutions use the Printed Circuit Board (PCB) technology, the multi-layer interconnects allowing for a reduction of stray inductances [11]. Main solutions are:

- replacement of wire bonding by a multi-layer flex substrate [12];

- replacement of wire bonding by a metal layer deposited on a thin insulating [13] (structure "SiPlit"); the authors show that the stray inductance is reduced compared to a wire bonded module (5.5 nH vs 11 nH)

- embedded dies in a printed circuit board [14]; with this solution, peripheral devices can be reported as close as possible to the power device; stray inductance lower than 1 nH is obtained.

Another approach is 3D integration where the chips are placed between two metallized ceramic substrates [15], which allow for an extraction of the heat through the both sides of the module [16-18]. A 40% reduction of the global thermal resistance [19] can be obtained with this solution. In [19], the parasitic inductances also remain low: 10 nH measured for a full converter, including power modules, busbars and decoupling capacitors.

As a conclusion, both solutions have their own advantages: PCBs allow for optimal integration of peripheral devices (for example decoupling capacitors) very close to the power dies, and ceramic substrates on both sides of the devices enhance heat dissipation. The proposed implementation of the PCoC module will take advantage of both technologies, using PCB to reduce stray inductances and ceramic substrates to improve heat dissipation.

B. Application to the PCoC module

Before the presentation of the chosen implementation principle, it has to be noted that, even if PCoC structure is of great interest for power devices having fast switching transients (i.e. for wide band gap components), the experimental study is carried out with silicon devices (IGBT and diode). In fact, due to their larger surface, they are easier to implement. In this paper, the electrical structure of the module is limited to a half-bridge. Thus, the module comprises two switching cells (Fig. 3a). Fig. 3b shows its realization principle. In order to simplify the comprehension, only one switching cell is drawn in this figure. A complementary 3D exploded view of the proposed implementation is given in Fig. 3c. The central plate shown in Fig. 2 is replaced by a multilayer printed circuit board (PCB) because it allows for simple electrical connections between the different parts of the module. It also permits to use classical (high voltage) SMD capacitors for the decoupling operation. The external plates are replaced by two direct bonded copper (DBC) substrates. Because they are good thermal conductors, these substrates are used for the thermal management of power dies. The cooling of the module is carried out using two cold plates.

In order to understand the electrical connections in the module, each electric potential is represented by a color in Fig. 3a and 3b: red for the positive potential of the DC bus ($+V_{DC}$), blue for the negative one ($-V_{DC}$), brown for the mid-point, and pink for the gate voltage. The 4-layers PCB is thus used to connect:

- the diode to the IGBT of the same switching cell,
- the DC-link and decoupling capacitors to the module; the busbar is therefore integrated directly in the power module allowing a reduction of the stray inductance,
- the mid-point of the half-bridge to the load,
- the gate driver to the IGBT chips.

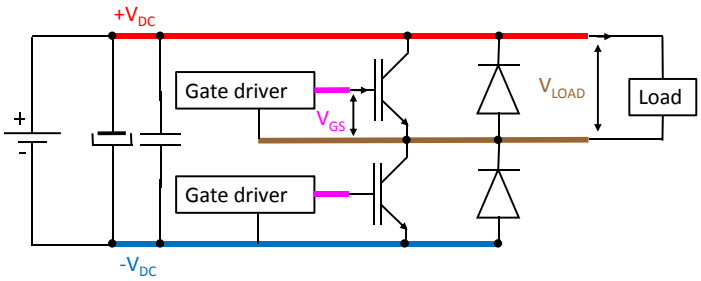
The reduction of the magnetic coupling between the power and gate circuits in a PCoC module is obtained by inserting the gate track in the central layers [7]. The central layers are also used to carry out measurements of the collector-emitter voltage of the IGBT during its turn-on and turn-off in order to evaluate the voltage as close as possible to the chip (not shown in Fig. 3). The top ($-V_{DC}$) and bottom layers ($+V_{DC}$), combined with both DBCs, act as a magnetic shield.

The presented structure includes therefore all the advantages of the basic PCoC structure presented in [7] and [8]: low stray inductance, no common mode capacitor, low electromagnetic interferences, gate-circuit not coupled to the power circuit, etc… However, this new implementation way has also many advantages:

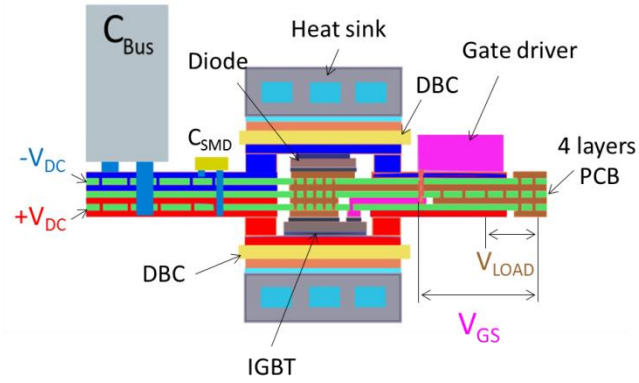
-the DBC permits an external electrical insulation between the dies and the heat sink,

-the decoupling capacitances are easily assembled and they are put as close as possible to the switching cell. Here, the use of a busbar like architecture permits to use classical SMD capacitances that offer the benefit of a high capacitance density and in the same time a very low stray loop inductance,

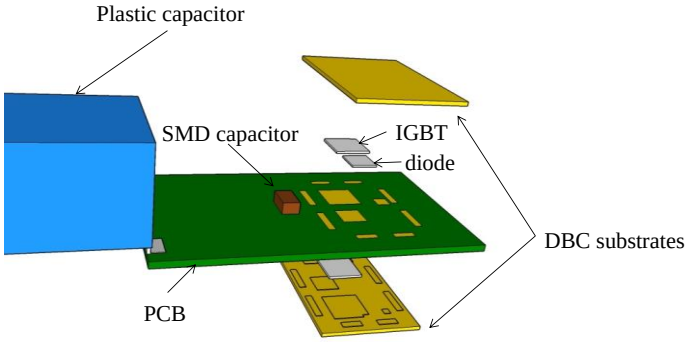
-the central plate is made with a PCB: measurement tracks are integrated in the multilayer structure, gate drivers could be easily reported on this PCB to realize an Intelligent Power Module.



a. Electrical Circuit



b. Principle of the implementation



c. 3D exploded view of the PCoC module

Figure 3. Presentation of the studied PCoC module.

III. INTEGRATION STEPS OF THE MODULE

A. *Silicon dies*

The IGBT dies are 5SMY 12M1280 (1200 V-150 A) from ABB. Their thickness is 140 µm. One main interest of these dies is the location of the gate pad in the corner. In fact, they can easily be integrated in a 3D package. Furthermore, this configuration permits an optical verification of the electrical connection between the gate pad and the corresponding copper track. For the diodes, we chose 600 V-200 A dies from Infineon (SIDC81D60E6). Their thickness is 70 µm.

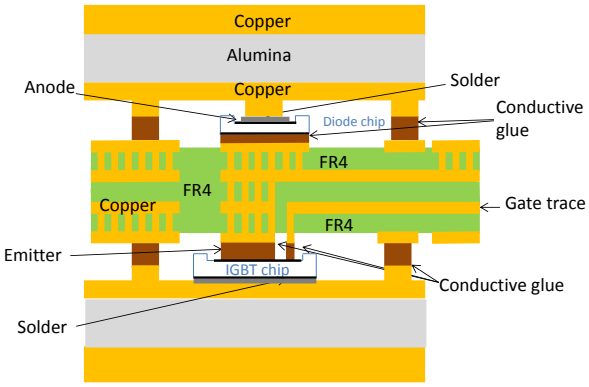
C. *Assembly principle of the power module*

Fig. 4 presents the assembly principle of the power module. The chips are soldered on the DBC substrate to insure a good thermal contact. The thermal property of the contact between the dies and the PCB is not a critical issue for this module because the cooler is placed on the other side of the chips. Conductive glue (EPO-TEK EK2000) is therefore used to simplify the realization. This silver-filled adhesive exhibits a good thermal (up to 20 $W.m^{-1}.K^{-1}$) and electrical conductivity. This glue is also used to connect the PCB to the DBC substrates. We used the glue as a "gap filler" material to make up for the difference in thickness between the IGBTs and the diodes (140 µm vs 70 µm).

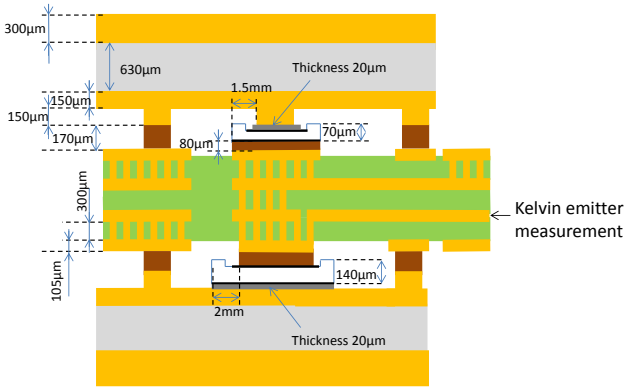
To provide a safe operation of the guard rings of the chips, a distance between the conductive material and the guard rings must be insured. In order to do this, the DBC substrates are chemically etched to form protruding features. In our case, the thickness of the copper of the DBC substrate is 300 µm and the etching depth is 150 µm. These protrusions also permit to connect the DBC substrates to the PCB to create a current path from the DC-link capacitor to the dies. They insure at least 150 µm of free space close to the guard rings.

On the PCB side (IGBT chip in Fig. 4.a), the free space between the guard rings and the metallic layer is insured by the PCB metallization (105 µm) and the first prepreg between the external metal layer and the first internal metal layer (300 µm), so it insures a spacing higher than 400 µm between the metal and the guard rings.

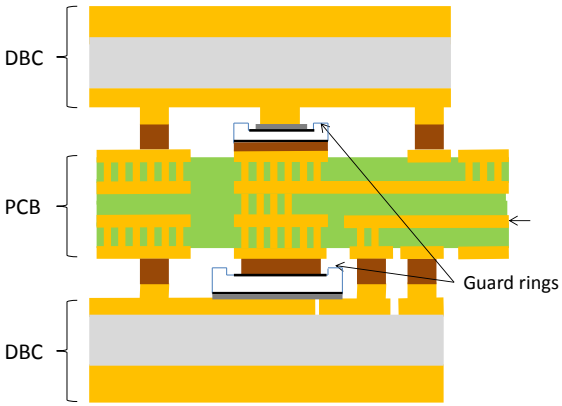
To obtain a good parallelism between the different substrates, the thicknesses of the glue between the IGBT chip and the PCB, between the diode chips and the PCB, and between the DBC substrate and the PCB are different. Note that the glue could be replaced by another die attach material, for example a solder.



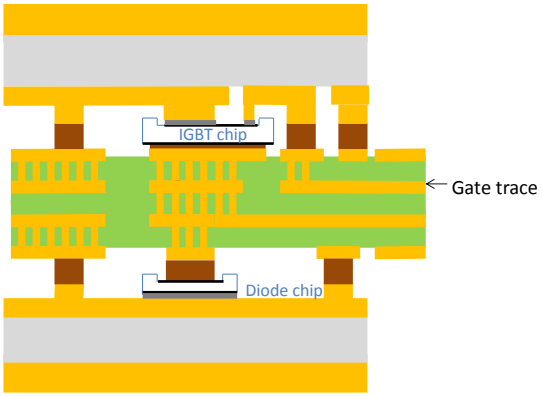
a. Cross section 1: gate trace



b. Cross section 2: Kelvin emitter measurement



c. Cross section 3: Kelvin collector measurement



d. Cross section 4: assembly of the second switching cell

Figure 4. Different cross sections of the power module

For the present realization, the actual layout of the final PCB (4 layers) are shown in Fig 5. The lines numbered 1 to 4 in this figure correspond to the position of the cross sections in Fig. 4. Photographs of the PCB and the DBC substrates prior to assembly are given in Fig. 6 and 7 respectively.

D. Technological steps

The soldering process is done in a vacuum oven (<5 mBar) to limit the oxidation of the copper plates and to reduce voiding in the soldering alloy. Tin-lead preforms (thickness 50 µm) and a solder flux are used to limit the tilt angle between the dies and the substrate. An additional weight of 4 g is placed on the dies during the soldering operation. The soldering profile is composed of 2 steps, a preheat step of 6 minutes at 140°C for solder flux activation, and a reflow peak of 1 minute up to 260°C for soldering operation. Both are performed under vacuum.

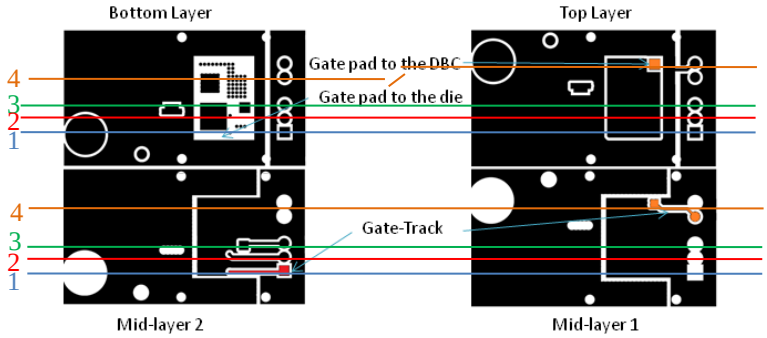


Figure 5. Layout of the PCB

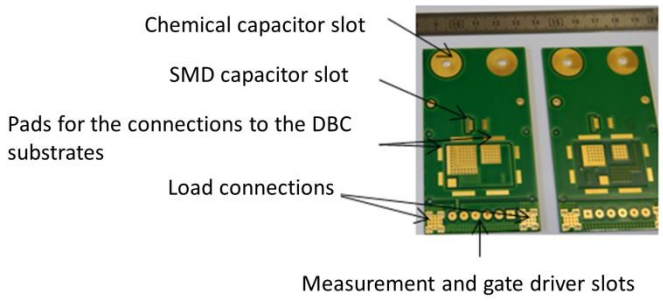


Figure 6. Top and bottom sides of the 4 layers PCB

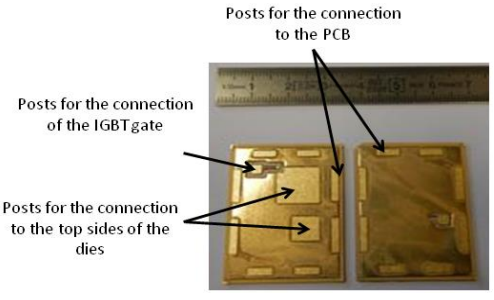


Figure 7. Top view of the DBC substrates after etching

The top side metallization of the dies used in this study being made with an Al-Si alloy, the soldering process is only possible after the selective deposition of another metal. Fig. 8 shows one

diode and one IGBT after the deposition of an Ni-Au layer. Masks are used during this deposition to protect the guard rings of the die.

The dies, the DBC substrates and the PCB have to be aligned during the reflow and the gluing processes. Two laser-cut ceramic jigs are thus used for this purpose: one to line-up the dies on the DBC substrate, the other one to line-up the DBC on the PCB (Fig. 9). These jigs are aligned using metallic dowel pins. Note that the use of relatively lighter materials compared to [8] permits to use a standard BGA equipment to perform this alignment process and to avoid the use of external parts (like plexiglas guides in [8]). With this equipment, the use of ceramic jigs can also be avoided.

When the assembly is finished, the electrical connections after soldering and gluing processes are optically verified with an ERSAScope side view camera (Fig. 10). Then, these connections are electrically tested. Finally, a dielectric gel is injected in the module to carry out electrical tests in switching conditions.

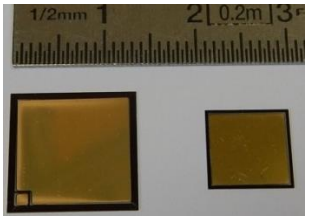


Figure 8. Top view of the dies after Ni-Au deposition

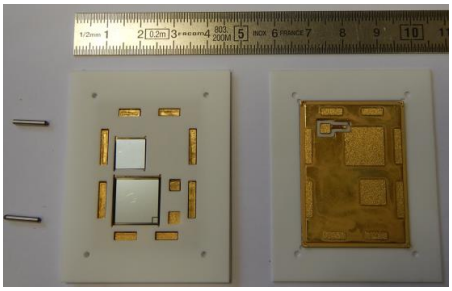


Figure 9. Picture of the ceramic jigs

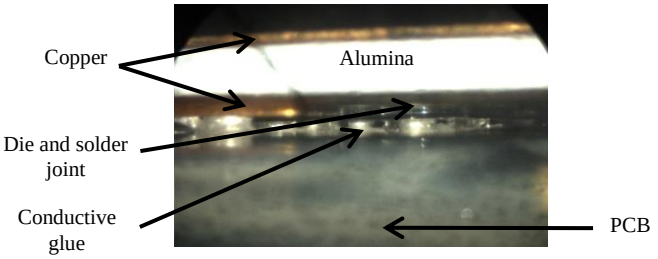


Figure 10. Side view of the top side of the PCoC assembly

IV. EXPERIMENTAL RESULTS

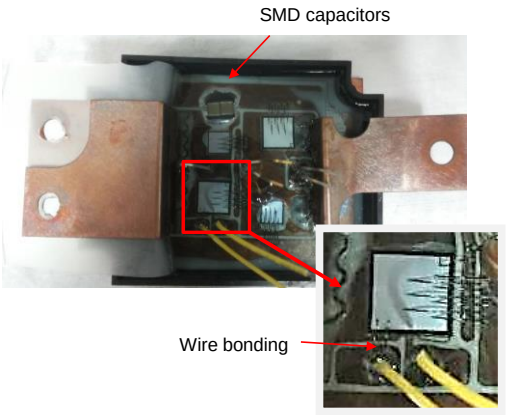
A. *Comparative study*

To compare the PCoC module stray inductance to that offered by the 2D classical approach, one planar module (Fig. 11) was realized with the same IGBT and diode chips by PRIMES innovation platform. Its electrical structure is also a half bridge. As seen in Fig. 11.a and 11.b, the module can be tested with and without internal decoupling SMD capacitors.

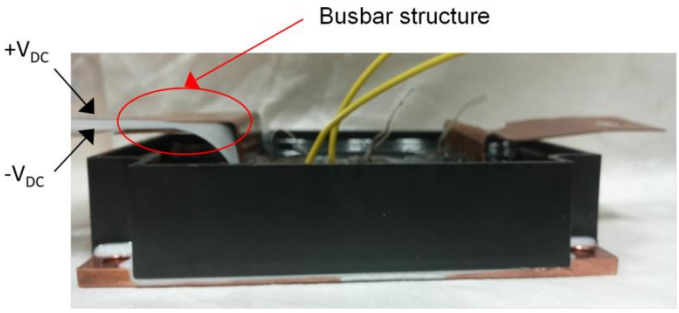
To evaluate the influence of the stray inductance in the switching cell, it is important to measure the collector-emitter voltage as close as possible to the IGBT chip. Fig. 11.b shows the chosen solution. A Kelvin voltage measurement is thus carried out via two posts situated on the DBC substrate: one post is directly linked to the collector electrode via the DBC metallization and the other one is connected to the emitter electrode via wire bonding. An effort was made to place these connecting wires (the "control" circuit) in the direction perpendicular to the current flow in the "power" circuit in order to reduce the magnetic coupling between them.

It has to be noted that the stray inductance due to lead frames is reduced as far as possible by creating a busbar structure which is directly soldered onto the DBC substrate (Fig. 11.c). This power module is therefore representative of the best planar power modules which can be realized with wire bonding.

a. Top view



b. Top view with decoupling SMD capacitors and details of the Kelvin collector-emitter measurement



c. Side view

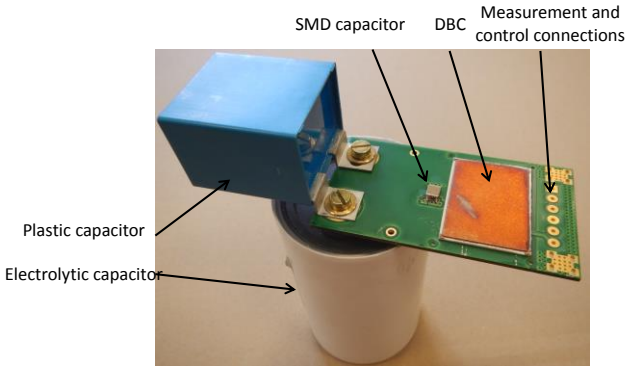
Figure 11. The planar module

B. Results

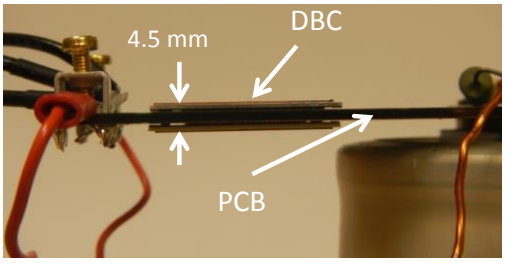
The planar and PCoC modules are tested in switching conditions based on the electrical circuit shown in Fig. 3a with an inductive load. They are connected to a DC link capacitor including an electrolytic capacitor and a plastic one (Fig. 12). The low side IGBT is continually open (-5 V on the gate-emitter voltage) and the high side IGBT is driven by a double pulse gate driver.

In this paper, each power module is tested without any internal decoupling capacitor and with two paralleled 220 nF SMD capacitors. The electrolytic and plastic decoupling capacitors are always present. The DC link voltage is 200 V and the load current is 20 A. No current sensor was integrated in the power modules, because they would have increased the stray inductance of the switching cells. Therefore, to have an acceptable comparison, the gate driver and the gate resistance are identical for each test.

Fig. 13 and 14 present respectively the switching waveforms of the collector-emitter voltage during IGBT turn-off and turn-on. The influence of the stray inductance can be seen in both figures. Fig. 13 shows that, during turn-off, the overvoltage is the highest for the planar module without SMD capacitor and the lowest for the PCoC module with SMD capacitors. Even if the overvoltage with the planar module is relatively low (<10 V), it is clear that the PCoC structure and the internal decoupling capacitors have beneficial effects on the stray inductance. The relatively low voltage spike during turn off is due to the use of classical IGBT dies that are quite slow. With very fast dies such as SiC MOSFETs, the voltage variation reduction between the planar and the PCoC modules will be more significant.



a. PCoC module V2



b. Side view of PCoC module V2

Figure 12. PCoC module connected to the DC link capacitor

The quantification of the benefits of the PCoC structure is easier during turn-on because the voltage variations due to the inductances are more obvious. In Fig 13, at t=80 ns, the voltage variation is respectively equal to 20 V, 14 V, 10 V and 4 V for the planar module without SMD capacitors, the planar module with SMD capacitors, the PCoC module without SMD capacitor and the PCoC module with SMD capacitors. Compared to the planar module without SMD, this corresponds to a reduction of 30%, 50% and 80% of the voltage drop at turn-on for the planar module with SMD, the PCoC module without SMD, and the PCoC module with SMD, respectively.

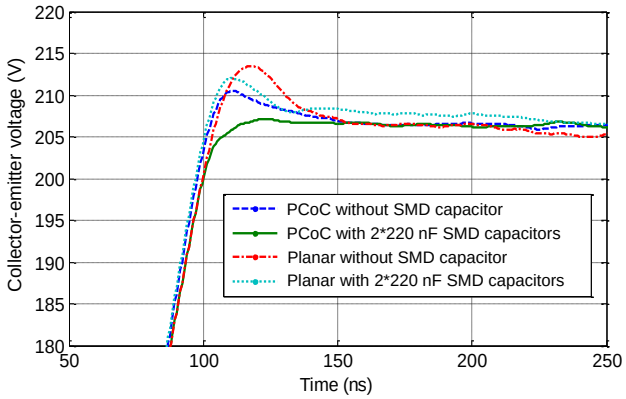


Figure 13. Waveforms during IGBT turn-off

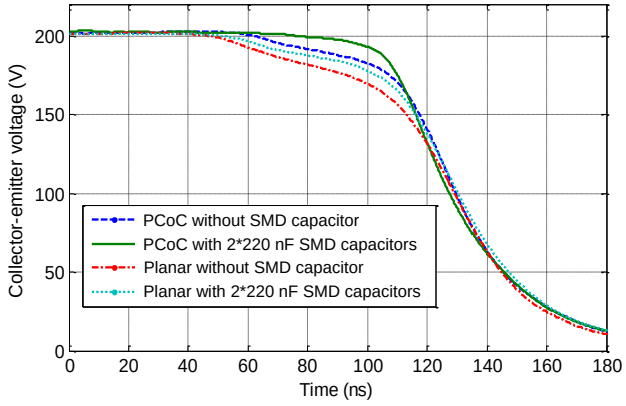


Figure 14. Waveforms during IGBT turn-on

In this example, the stray inductance of the PCoC module without SMD capacitor is lower than this of the planar module including internal decoupling capacitors. The voltage drop during turn-on is 5 times lower in the case of the PCoC module with SMD capacitor than in the case of a relatively good planar module (with a busbar directly connected to the DBC substrate). In consequence, it can be concluded that the PCoC module has a very good behavior in term of stray inductance.

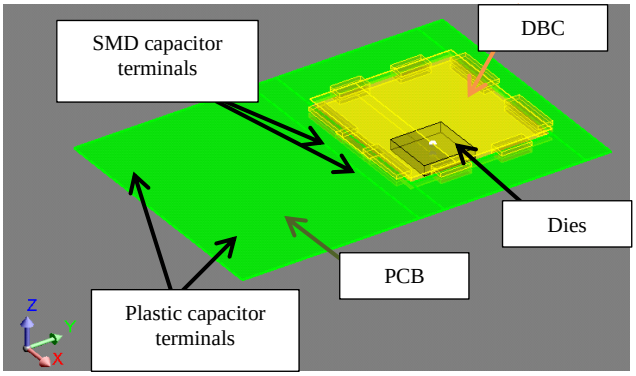
This study also shows the importance of the integration of the decoupling capacitor in the PCoC assembly to reduce the stray inductance of the switching cell. In fact, the results presented in [8] already demonstrated that the PCoC structure was better than the planar one. With these new results, it is clear that the easy integration of the decoupling capacitor on the PCB is a major advantage of the new assembly proposed in this paper: without this capacitor, the decrease of the stray inductance would not be significant compared with the best planar modules (including decoupling capacitors).

V. ANALYSIS

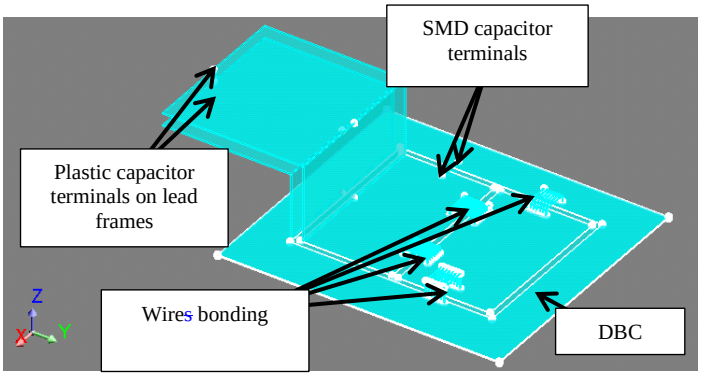
A. Simulation study

Simulations are carried out to analyze the experimental waveforms of Fig. 13 and 14. Estimation of stray inductances of both planar and PCoC modules are performed with the InCa3D software (Fig. 15) based on the PEEC (Partial Element Equivalent Circuit) method. Note that only two chips (one IGBT of the upper side of the module and one diode of the lower one) are used in these simulations. Indeed, only one IGBT and one diode are involved for a given output current direction, the other devices being biased negatively. Due to geometrical symmetries, the stray inductance value of the first switching cell is equal to the other one.

Based on the geometry presented in previous sections, InCa3D software allows for a calculation of the stray inductance value of the switching cell. First, the global inductance between both SMD capacitance terminals is estimated. In the case of the PCoC module, the calculated value is 0.45 nH. Then, a calculation of the global inductance between plastic capacitor terminals is carried out (without SMD capacitor). For the PCoC module the stray inductance values is 0.5 nH and, for the planar one it is 11 nH.



a. PCoC module



b. Planar module

Figure 15. *Simulated geometry (InCa3D)*

B. Comparison between experimental and simulation results

In the case of the PCoC module, a direct comparison between experimental and simulation data could lead to a wrong analysis: the stray inductance without SMD capacitor is only increased by 10% whereas the increase of the overvoltage is far greater (Fig. 13). In fact, SMD and plastic capacitors have their own equivalent series stray inductances (ESL). These values can be obtained with manufacturer datasheets. The ESL of SMD capacitors is 1 nH leading to a global stray inductance of the switching cell close to 1.5 nH. In the case of the plastic capacitor, the ESL is 10 nH. The total inductance of the power loop without SMD capacitor is therefore close to 10.5 nH.

In the case of the planar module, the stray inductance including the plastic capacitor ESL (10nH) is above 21 nH. It is in good accordance with experimental results: without SMD capacitor, the over-voltage with planar module is about two times higher than the one with PCoC module (without SMD capacitor).

As a conclusion, taking into account ESL values and assuming that current switching speeds are almost identical in both case, there is a good accordance between experimental and simulation results: in Fig. 13, the overvoltage is 5 V without SMD capacitors and less than 1 V with them.

With faster components like silicon carbide MOSFETs, the reduction of the overvoltage should be even larger. In fact, current variation di/dt during turn-off of SiC MOSFETs was measured or evaluated by authors. For illustration, values of 3750 A/µs or 5000 A/µs were given respectively by Wang et al [22] and Toyoshima et al [23] for 1200 V / 100 A MOSFETs. If the stray inductance of a planar module is considered to be close to 20 nH and di/dt close to 5000 A/µs, the corresponding over-voltage is 100V. In the same condition, the over-voltage in a PCoC module with internal decoupling capacitor is reduced to only 7.5 V (stray inductance close to 1.5 nH).

This study also recalls that the use of low stray inductance power modules in optimal conditions necessarily involves the use of capacitors with low ESL. In that sense, the use of PCBs allowing for easy implementation of SMD capacitors close to the chips is a good alternative.

C. Limits of this study

Both experimental and simulation results presented above show the interest of the PCoC structure to obtain very low stray inductances in switching cells. However, this power module structure may appear complicated regarding technological realization. Therefore, three complementary studies have to be carried out for future industrial developments:

- reduction of common mode currents compared to other solutions has to be demonstrated,
- heat dissipation has to be characterized and compared with other modules,
- reliability has to be demonstrated.

Concerning common mode currents, the results from Yao et al. [9] are really encouraging. About thermal aspects, the main remaining question is about the thermal contact resistance between the front side of the chips and DBC substrates which could reduce heat transfer capabilities of this solution. In fact the area of anode, source or emitter electrodes can be largely lower than total chip area, especially for small dies like SiC MOSFETs.

Concerning implementation, the proposed assembly has to be modified, for example, replacing the conductive glue by

sintering or brazing technologies. Other solutions based on embedded dies can also be envisaged [21].

D. Reliability aspects

Reliability is a key issue for power electronics packaging, as it has to ensure long operating life, while enduring harsh environmental conditions (thermal cycling, high temperature, etc.). Many parameters have an impact on reliability: some are related to the design (use of PCB, of materials with lower CTE or more compliant, thickness of the various layers…). Some are related to the manufacturing process (voids in the solder, soldering profile, lamination of the PCB layer…).

Regarding PCB, a rigid material with a CTE larger than that of the ceramic substrates is probably not the best option from a reliability point of view. However, many PCB materials are available, some with lower CTE, some which can operate at higher temperature. It must be noted that many research groups work on embedding power semiconductor dies within the PCB, and that although this is fairly recent no major reliability issue was reported yet [24].

This paper is focused on PCB because of the easy access to the technology, and because multilayer PCB allows producing the laminar structure required. Next developments should focus on matching the various materials in the structure, not only from an electrical point of view, but also on other aspects such as thermal, thermo-mechanical, etc. This should indicate whether PCB is suitable, or if other materials (flex substrate, rigid-flex hybrid boards, multilayer LTCC…) should be used.

VI. CONCLUSION

This paper firstly introduces the Power Chip-on-Chip concept and its main advantages especially for very high-speed components such as SiC MOSFETs. After this, we mainly focus on the implementation of the PCoC concept using PCB and DBC materials.

Experimental tests in switching conditions, confirmed by electromagnetic simulations, show that the stray inductance is drastically reduced when using a PCoC module compared with planar ones, especially when internal SMD decoupling capacitors are integrated in the assembly. With faster dies, for example SiC MOSFETs, the reduction of the overvoltages should be even larger than the results presented in this paper. In some cases, the lower overvoltages caused by a PCoC module could allow to use power devices with a lower voltage rating (and therefore a lower on-stage voltage drop), closer to the actual DC link voltage. Therefore, the switching energies and the on-state voltages could be reduced, which would induce a better global efficiency of the power converter.

This paper has validated the concept of using a PCB as central plate for a PCoC module. However, the characterization of the module in steady state conditions must be carried out, to evaluate the advantage of the PCoC module regarding common mode current reduction, but also to make sure that the die stacking configuration is compatible with an efficient thermal management.

ACKNOWLEDGMENT

Authors would like to thank the Carnot Institute “Energies du Futur” and the Région Rhone-Alpes for their financial support.

REFERENCES

[1] F. Xu, T.-J. Han, D. Jiang, L.-M. Tolbert, F. Wang, J. Nagashima, S.-J. Kim, S. Kulkarni and F. Barlow, “Development of Sic JFET-Based Six Pack Power Module for a Fully Integrated Inverter”, *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1464 - 1478, March 2013.

[2] Z. Xu, D. Jiang, M. Li, P. Ning, F. Wang and Z. Liang, “Development of Si IGBT Phase-Leg Modules for Operation at 200 ˚C in Hybrid Electric Vehicle Applications”, *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5557 - 5567, December 2013.

[3] Z. Qiu, H. Zhang and G. Chen, “Study and design of Noninductive busbar for high power switching converter”, *IEEE 5th International on Power Electronics and Motion Control Conference*, 2006.

[4] K. Xing, F.-C. Lee and D. Boroyevich, “Extraction of Parasitics within Wire-Bond IGBT Modules”, *13th Annual Applied Power Electronics Conference and Exposition*, 1998.

[5] J.-N. Calata, J.-G. Bai, L. Xingsheng, W. Sihua and G.-Q. Lu, “Three-Dimensional Packaging for Power Semiconductor Devices and Modules”, *IEEE Transactions on Advanced Packaging*, vol. 28, pp. 404 - 412, August 2005.

[6] C. Gillot, C. Schaeffer, C. Massit and L. Meysenc, “Double-sided cooling for high power IGBT modules using flip chip technology”, *IEEE Transactions on Components and Packaging Technologies*, vol. 24, pp. 698 - 704, December 2001.

[7] E.Vagnon, P-O. Jeannin, J-C. Crebier, Y. Avenas, ”A Busbar Like Power Module Based On 3D Chip On Chip Hybrid Integration”, *IEEE Transactions on Industry Applications*, Volume 46, pp. 2046-2055, 2010.

[8] J.-L. Marchesini, Y. Avenas, P.-O. Jeannin, S. Boulahrouz, “Reduction of the Stray Inductance in a Switching Cell Using the Power Chip-On-Chip 3D Integration Concept”, *Conversion Congress and Exposition (ECCE)*, Raleigh, 2012.

[9] C. Yao, W. Li, H. Li, C. Han, M. Wang, J. Qian, X. Zhang, F. Luo, J. Wang, “Common-mode noise comparison study for lateral wire-bonded and vertically integrated power modules”, *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.3092-3098, 20-24 Sept. 2015

[10] O. Goualard, N. Videau, T.-B Doan, T. Lebey, V. Bley, T. Meynard, “Integrated Screen Printed Capacitors in a GaN DC-DC Converter Allowing Double Side Cooling”, IEEE Electronics System-Integration Conference, 2014.

[11] Y. Ikeda, Y. Iizuka, Y. Hinata, M. Horio, M. Hori, Y. Takahashi, “Investigation on wirebond-less power module structure with high-density packaging and high reliability”, *IEEE 23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp.272-275, 23-26 May 2011

[12] T. Stockmeier, P. Beckedahl, C. Gobl, T. Malzer, “SKiN: Double side sintering technology for new packages”, *IEEE 23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2011, pp. 324-327

[13] K. Weidner, M. Kaspar, N. Seliger, “Planar Interconnect Technology for Power Module System Integration”, *7th International Conference on Integrated Power Electronics Systems (CIPS)*, 2012, pp. 1-5.

[14] E. Hoene, “Ultra Low Inductance Package for SiC”, *ECPE workshop on power boards*, 2012.

[15] L. Zhenxian, P. Ning, F. Wang, L. Marlino, “Planar bond all: A new packaging technology for advanced automotive power modules”, *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.438-443, 15-20 Sept. 2012.

[16] L-D. Stevanovic, R-A. Beaupre, A-V. Gowda, A-G. Pautsch, S-A. Solovitz,, “Integral micro-channel liquid cooling for power electronics”, *Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp.1591-1597, 21-25 Feb. 2010.

[17] R. Riva, C. Buttay, M-L. Locatelli, V. Bley, B. Allard, “Design and Manufacturing of a Double-Side Cooled, SiC based, High Temperature Inverter Leg”, *Proceedings of the High Temperature Electronics Conference and Exhibition, HiTEC 2014*, 2014.

[18] H. Zhang, S-S. Ang, H-A. Mantooth, S. Krishnamurthy, “A high temperature, double-sided cooling SiC power electronics module”, *2013 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp.2877-2883, 15-19 Sept. 2013.

[19] C. Buttay, J. Rashid, C. Mark Johnson, P. Ireland, F. Udrea, G. Amaratunga, R. Malhan, “High performance cooling system for automotive inverters”, *Proc. European Conference on Power Electronics and Applications, EPE*, 2007, pp. 1-9.

[20] S. Ji, D. Reusch and F.-C. Lee, “High-Frequency High Power Density 3-D Integrated Gallium-Nitride-Based Point of Load Module Design”, *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4216 - 4226, September 2013.

[21] G. Regnat, P-O. Jeannin, G. Lefevre, J. Ewanchuk, D. Frey, S. Mollov, J-P. Ferrieux, “Silicon carbide power chip on chip module based on embedded die technology with paralleled dies”, 2015 IEEE Energy Conversion Congress and Exposition (ECCE), pp.4913-4919, 20-24 Sept. 2015.

[22] G. Wang, F. Wang, G. Magai, Y. Lei, A. Huang and M. Das, "Performance comparison of 1200V 100A SiC MOSFET and 1200V 100A silicon IGBT," Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, Denver, CO, 2013, pp. 3230-3234.

[23] S. Toyoshima, S. Hatsukawa, N. Hirakata, T. Tsuno, Y. Mikamura, “Compact SiC Power Module for High Speed Switching”, SEI TECHNICAL REVIEW, no 80, pp. 81-84, 2015

[24] A. Ostmann, L. Boettcher, D. Manessis, S. Karaszkiewicz, K-D. Lang, “Power modules with embedded components”, Microelectronics Packaging Conference (EMPC) , 2013 European, pp. 1-4, 2013.